PowerVR SGX Series5
IP Core Family

The PowerVR™ SGX Series5 Graphics Processing Unit (GPU) IP core family is a series of highly efficient graphics acceleration IP cores that meet the multimedia requirements of the next generation of consumer, communications and computing applications.

PowerVR SGX Series5 architecture is fully scalable for a wide range of area and performance requirements, enabling it to target markets from low cost feature-rich mobile multimedia products to very high performance consoles and computing devices.

The family incorporates the revolutionary Universal Scalable Shader Engine (USSE™), with a feature set that exceeds the requirements of OpenGL 2.0 and Microsoft Shader Model 3, enabling 2D, 3D and general purpose (GP-GPU) processing in a single core.

PowerVR SGX Family

Series5XT	SGX543MP1-16, SGX544MP1-16, SGX554MP1-16
Series5	SGX520, SGX530, SGX531, SGX535, SGX540, SGX545

Multi-standard API and OS Support

Embedded APIs	OpenGL ES 2.0 and OpenGL ES 1.1 OpenVG 1.1 OpenCL 1.1 OpenWF
Desktop APIs	DirectX9 (SGX535/545) and DirectX10.1 (SGX545) OpenGL 2.1 (SGX535/545) and 3.1 (SGX545)
OS Support	Linux, Symbian and Android Microsoft WinCE and Windows Desktop RTOS on request

Features

- Most comprehensive IP core family and roadmap in the industry
- Series5 shader-driven tile-based deferred rendering (TBDR) architecture
- Fully programmable GPU using unique USSE architecture
- Support for all industry standard mobile and desktop graphics APIs and operating sytems
- Fully backwards compatible with PowerVR MBX

Benefits

- Extensive product line supports all area/performance requirements
- Low risk solution for all embedded graphics applications
- Shader-based architecture enables near photo realistic image quality
- Fully compliant proven implementations of all APIs
- Lowest power consumption and silicon footprint
- Low host CPU and memory system bandwidth load

Applications

- Smart and feature phones
- Mobile internet devices (MIDs)
- Personal media players
- Games consoles
- HDTV and set-top boxes
- Personal navigation devices
- In-car navigation and information
- Electronic dashboards
- UMPCs, laptops and netbooks

Comprehensive Roadmap

PowerVR SGX cores offer the widest range of performance/area options, so that the optimal solution is available for every set of application requirements.

PowerVR Series5 shader-driven TBDR architecture

Unique, patented tiling technology enables on-chip processing of hidden surface removal (pixel perfect and submission order independent) and pixel blending. This enables deferred shading, eliminating all unnecessary access to off-chip memory and assuring that shader cycles only process visible shader effects.

The decoupling of geometry and vertex processing from shader-based rasterization enables higher throughput while maximizing tolerance to system latencies. Hardware-based perfect tiling and culling algorithms, used in combination with seamless scene complexity management and compression, enable PowerVR SGX to handle arbitrarily complex scenes in limited memory footprints with the lowest memory bandwidth usage.

Programmable USSE

USSE is a scalable multi-threaded multimedia processing engine that efficiently enables advanced geometry and pixel processing including procedural geometry and textures, advanced per pixel and vertex lighting effects as well as other related GP-GPU tasks (e.g., physics, video and image processing). These tasks are automatically broken down into processing packets which are then scheduled across a number of multi-threaded execution units in the USSE. The USSE enables optimal hardware load balancing, maximum latency tolerance and efficient gate use, all accessed through a single software programming model and compiler.

For maximum efficiency, additional hardware engines, including texture, pixel and tiling accelerators work alongside the USSE in the PowerVR SGX architecture.

USSE enables up to IEEE 754 single precision floating point data processing essential for the best possible image quality and vital for effective GP-GPU multimedia processing.

An advanced microkernel based approach to scheduling assures maximal performance at minimal CPU load and enables extremely rapid context switching and concurrent multi-API support.

Low Power

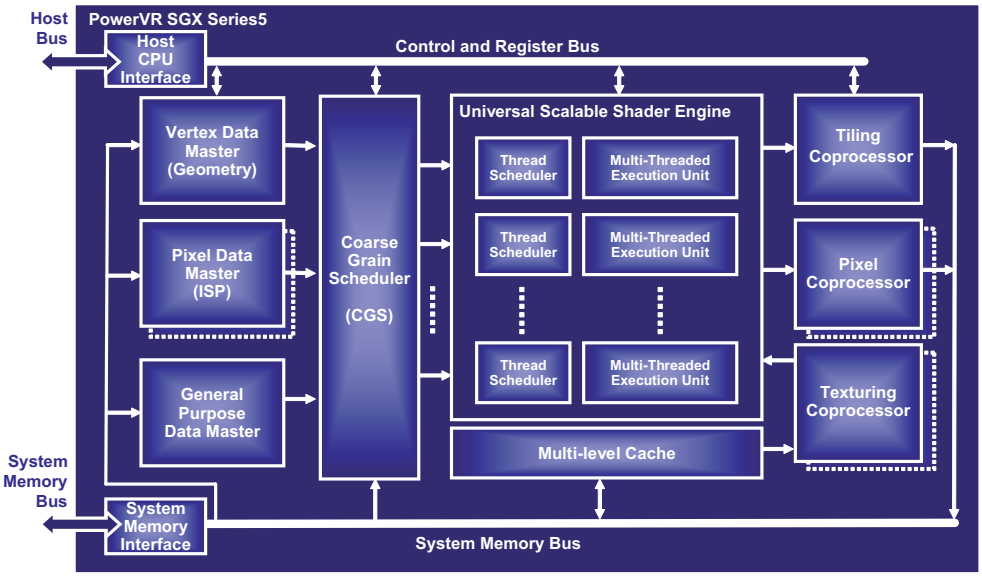
PowerVR SGX Series5 cores are built on a foundation of unique patented technologies that deliver class leading performance while keeping power dissipation to a minimum. PowerVR's inherently low-power architecture is complemented by the use of the latest sophisticated clock gating techniques to ensure the lowest active and standby power consumption.

High Performance per mW

The PowerVR SGX Series5 IP core family currently comprises six variants scalable for a range of area and performance requirements to accommodate the needs of many target markets. Performance scales with clock speeds up to 400 MHz and beyond.

System Level Cache Option

A range of pre-verified system level cache configurations (32, 64 and 128KB) are available to further reduce the bandwidth usage and maximize latency tolerance through access profile optimized caching.



Imagination

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