PowerVR Series6
IP Core Family

PowerVR® Series6 is the latest GPU (Graphics Processing Unit) IP core family that sets a new standard for high performance, ultra-low power graphics, scalable for markets from mobile and tablet to high-end gaming and computing.

Series6 is based on the innovative PowerVR 'Rogue' architecture which builds on the maturity and unrivalled success of the previous five generations of PowerVR GPUs. It enables devices to deliver amazing user experiences, from innovative 'natural' user interfaces to ultra-realistic gaming, as well as enabling previously unachievable applications from advanced content creation and image processing to sophisticated augmented reality and environment-aware solutions. The Series6 feature set meets or exceeds the requirements for APIs such as OpenGL ES 3.0, OpenCL 1.1 EP and DirectX 9_3/10_0 and supports all major operating systems.

Based on a scalable number of compute clusters, the PowerVR Series6 architecture is designed to target the requirements of a growing range of demanding markets from mobile to the highest performance embedded graphics including smartphones, tablets, PC, console, automotive, DTV and more. The Series6 USC (Unified Shading Clusters) are designed to offer high performance and efficiency while minimising power and bandwidth requirements.

Delivering the best performance in both GFLOPS/mm^2 and GFLOPS/mW, PowerVR Series6 GPUs can deliver 20x or more of the performance of current generation GPU cores targeting comparable markets. This is enabled by an architecture that is around 5x more efficient than previous generations.

PowerVR Series6 Family

G6100, G6200, G6230, G6400, G6430, G6630

Multi-standard API and OS Support

Embedded APIs	Khronos OpenGL ES 1.x/2.0/3.0 Khronos OpenCL 1.1/1.2 EP Android Renderscript/Filterscript
Desktop APIs	Khronos OpenGL 3.2 Microsoft DirectX 9_3 (G6100) and 10_0 (G6200, G6230, G6400, G6430, G6630)
OS Support	Linux, Android, Microsoft WinEC, Windows 8 and Windows RT

Features

- Most comprehensive IP core family and roadmap in the industry
- Series6 tile-based deferred rendering (TBDR) architecture featuring unified shaders
- Fully programmable GPU using unique USC architecture
- Support for all industry standard mobile and desktop graphics and compute OS and APIs
- Fully backward compatible with PowerVR SGX™ cores

Benefits

- Extensive product line supports all area/power/performance points
- Proven technology that provides a low risk solution for all embedded graphics applications
- Industry-leading ecosystem and developer community
- Fully compliant, proven implementations of all APIs
- Unified shader-based architecture enables the highest efficiency and performance in the industry
- Lowest power and area for a given performance envelope
- Low host CPU and memory system bandwidth load

Applications

- Smart and feature phones
- Mobile internet devices (MIDs)
- Personal media players
- Games consoles
- Smart TV and set-top boxes
- Personal navigation devices
- In-car navigation and information
- Electronic dashboards
- UMPCs, laptops and netbooks
- Connected home

Comprehensive Roadmap

Alongside the PowerVR Series5 (SGX) family, the Series6 cores allow Imagination Technologies® to offer the widest range of performance/power/area options, so that the optimal solution is available for every set of application requirements.

PowerVR Series6 Shader-Based TBDR Architecture

Unique, patented tiling technology enables on-chip processing of hidden surface removal (pixel perfect and submission order independent) and pixel blending. This enables deferred shading, eliminating all unnecessary access to off-chip memory and ensuring that shader cycles only process visible shader effects.

The decoupling of geometry and vertex processing from shader-based rasterization enables higher throughput while maximizing tolerance to system latencies. Hardware-based perfect tiling and culling algorithms, used in combination with seamless scene complexity management and compression, enable PowerVR Series6 to handle arbitrarily complex scenes in limited memory footprints with the lowest memory bandwidth usage.

Highly Scalable, Programmable Processing Clusters

The USCs are multi-threaded processing units that are optimised for the operations used in vertex and pixel shaders and also practical GPU compute tasks (video and image processing, for example). The USC architecture is highly scalable, meaning that multiple clusters can be implemented with very little overhead (performance scales almost linearly with additional clusters).

The unified architecture combined with intelligent task scheduling and hardware load balancing means that processing resources achieve maximum utilisation and latency tolerance.

Optimised data paths and local caching enable increased performance efficiency while reducing power consumption.

Low Power, High Performance, Ultimate Efficiency with PowerGearing

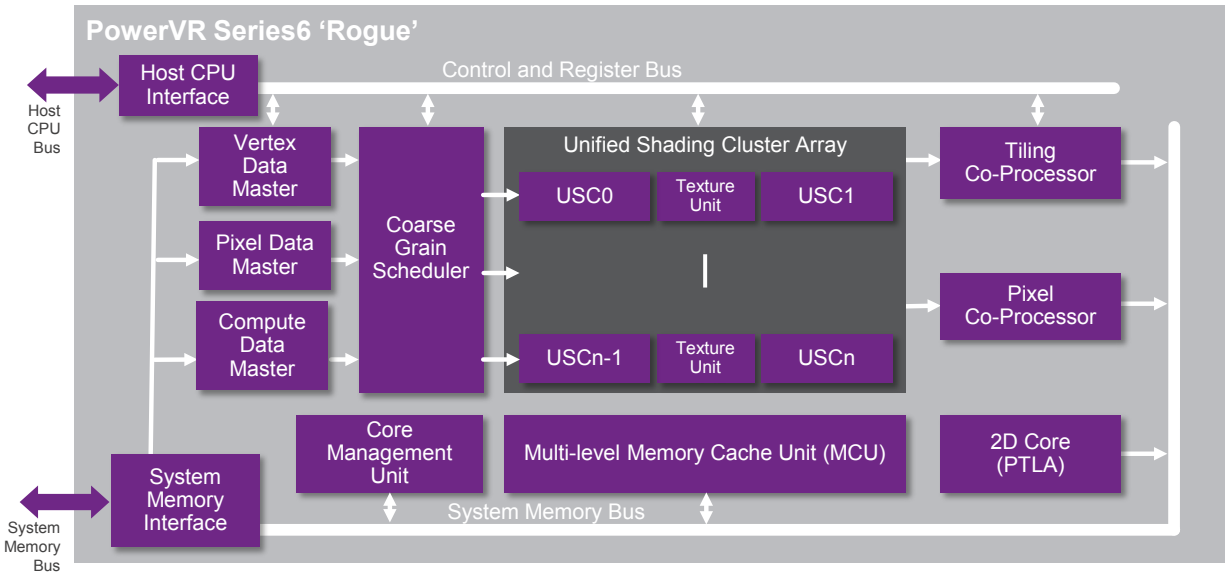
From the outset the PowerVR Series6 cores were designed with high performance and low-power consumption in mind. Precision, feature set and performance are balanced carefully versus the practical requirements of the embedded market. The patented PowerVR technologies such as Hidden Surface Removal (HSR) mean that the cores are inherently efficient at an architectural level and this is complemented by features such as multi-level clock gating, support for power islands and PowerGearing™ advanced power management.

Triple Compression for lowest bandwidth

The PowerVR 'Rogue' architecture offers triple compression including lossless geometry compression (to manage the increasing geometry complexity of scenes), market leading lossy PVRTC™ (to handle increasing texture counts and sizes) and lossless framebuffer compression (to handle system level bandwidth due to the ever increasing size of render targets both on-screen and off-screen). Reduced bandwidth results in an overall improvement in system efficiency and reduced power consumption.

Microkernel flexibility

The PowerVR 'Rogue' architecture is driven by a software microkernel running on a C-programmable microcontroler thus ensuring minimal host CPU load with maximal flexibility by managing all GPU events locally. The microkernel enables low-latency power management through direct handshake signals with SoC-level power management and DVFS control blocks.



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