

PowerVR Video Encoder

IP Core Family



PowerVR™ Video Encoder IP cores are multi-standard SD and HD video encoders, available as synthesiable RTL. The cores encode video from raw image data, producing a compliant bit stream in one of several supported formats.

H.264 is fully supported, including HP, MP and BP as well as MVC for stereoscopic encoding. The broad support of the H.264 feature set enables an encoder, that offers the highest quality, in the lowest bitrates. Additionally, 10-bit, 4:2:2, 4:4:4 and H.264 lossless profiles allow for high quality encoding maintaining the original source material quality, ideal for applications including wireless display.

The inclusion of support for VP8/WebM makes the cores ideal for WebRTC applications, and other video conferencing applications.

The multistream capability of the cores, and support of the H.264 MVC standard (as used by Blu-ray 3D) make the PowerVR video encoder family ideal for stereoscopic applications. The ability to encode in MPEG-2 makes the encoder suitable for DLNA applications.

Features

- Programmable stream manager for header generation and flexible rate control
- Advanced, highly efficient motion search algorithm
- Dedicated hardware encoding
- CABAC and CAVLC
- Scalable architecture
- B-Frames
- Flexible rate control:
 - CBR
 - VBR
 - Const Qp
 - Low delay
- Automatic hardware power management

Benefits

- Wide range of video standards supported
- Low power consumption
- High quality compression
- Low host-CPU processing requirement
- Silicon efficient area
- 4K high frame rate support
- H.264 MVC for Stereoscopic S3D

Applications

- Mobile (phones and tablets)
- Surveillance
- Automotive
- Transcoding
- DSC & DSLR
- Wireless display
- WebRTC
- Video Conferencing

Comprehensive standards support

Standard	Resolution	Frame Rate
H.264 HP @ L5.1	3840 x 2160	30
VP8	1920 x 1080	30
H.264 HP @ L4.2	1920 x 1080	60
H.264 MVC @L4.1	1920 x 1080 x 2	24fps Left 24fps Right
MPEG-4 SP	720 x 480	30
H.263	352 x 288	30
JPEG	16 mpixels	100 mpixels/s
MPEG-2 MP @ ML	720 x 480	40

Stream Manager

PowerVR video encoders contain a stream manager, based on an internal Imagination MCU which performs all header encoding and rate control allowing the cores to provide compliant bit streams. The stream manager also provides control for the multi-mode hardware modules. This embedded Imagination MCU core offloads processing requirements from the host CPU.

Motion Search Algorithm

The advanced search algorithm allows a large effective area to be searched, ensuring the highest quality compression is achieved, while minimizing memory bandwidth requirements.

Low Power Consumption

Advanced automatic hardware power management techniques including block and register level clock gating ensure that the minimum amount of logic is powered for each video standard. This ensures that the cores have frugal power requirements enabling high performance, real-time video encode to be brought to power constrained devices such as portable media players and mobile phones.

Scalable Architecture

PowerVR video encoder architecture is scalable to enable area/performance trade-offs allowing for small core sizes or high frame rate/resolution encoding.

M-JPEG/JPEG Encoding

The cores provide full encoding outputting a JFIF1.1 compliant format suitable for use in mobile applications.

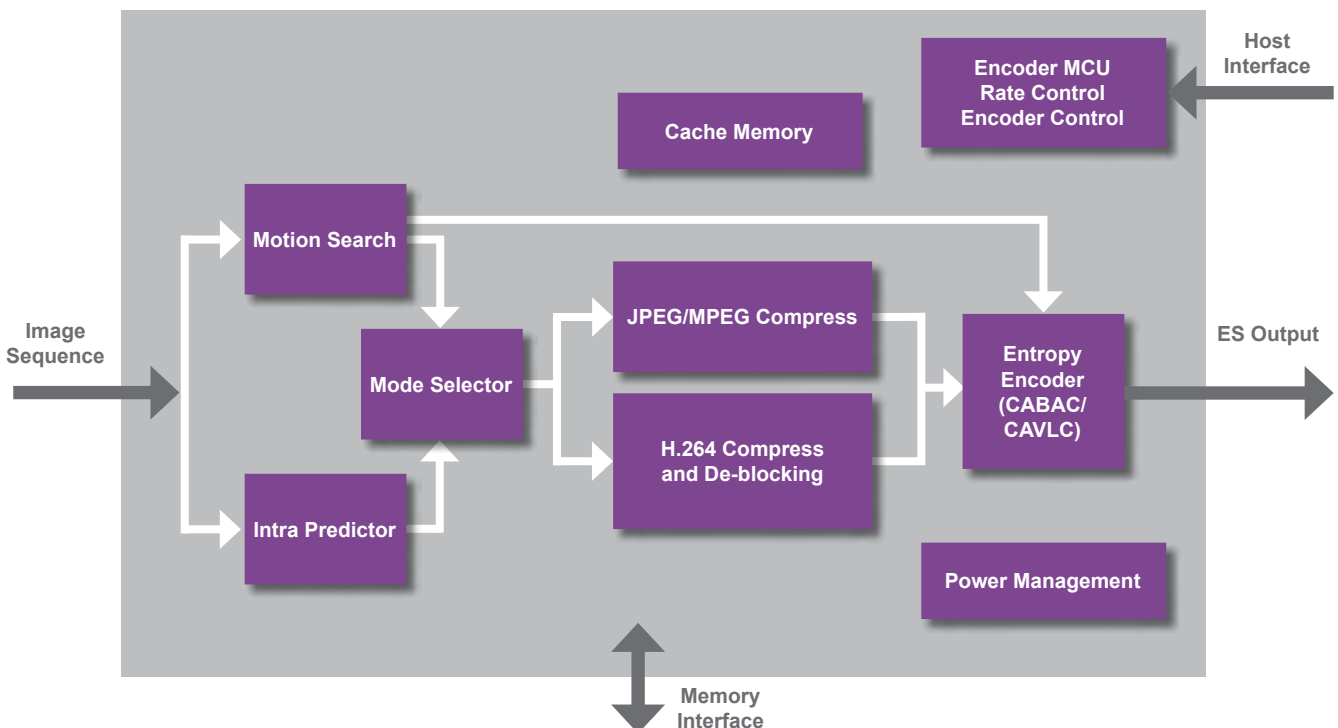
Software Support

PowerVR video encoders have low overhead host CPU software drivers supporting the video standards through a single easy to use application programming interface. OpenMAX IL drivers are a standard deliverable. The drivers are in ANSI C Code and are easily ported to a wide range of operating systems. The firmware for the stream manager is provided as part of the product deliverables.

Ease of Integration

All our IP platforms are designed to be easily integrated into a wide range of SoCs. They are system latency tolerant, with low memory bandwidth loading and excellent power management.

PowerVR Video Encoder Architecture



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